Development of
with PC104plus

a Pipeline CAMAC controller single board computer

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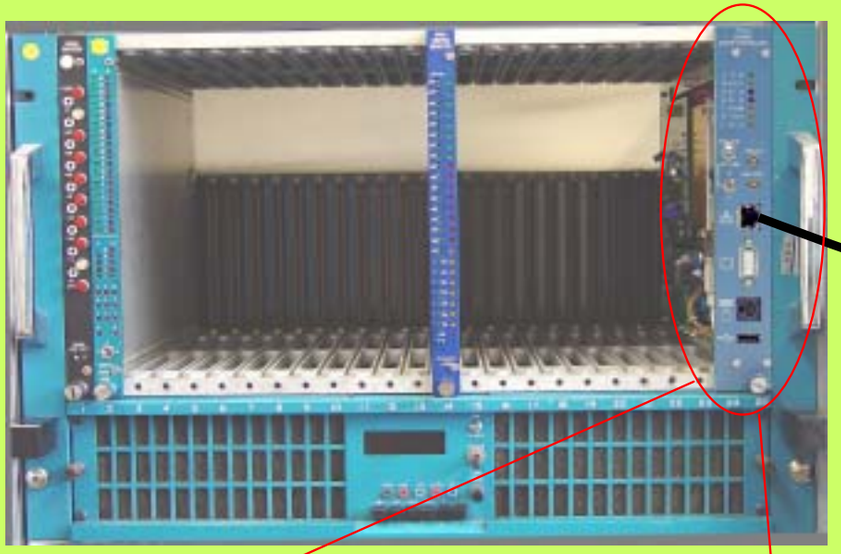
Abstract

A pipeline CAMAC controller with PC/104-Plus single board computer has been developed. The architecture of the pipeline CAMAC controller is completely different from that of traditional CAMAC controller. The pipeline CAMAC controller adopted truly pipelined command and data paths from/to computer memory to/from CAMAC. The pipeline method enabled the controller maximum speed of CAMAC, approximately up to 3 MB/sec with 24-bit data. The controller also has a DAQ function such as event numbering for co-existence with other equipment such as VME.

Not only the functionality and the performance but also the pipeline architecture and the design concept are described.

Overview of Pipeline CAMAC controller



Fast Ethernet

PC104plus PC board computer
PCM-9370's Crusoe TM5400, Memory, Flash Disk, Ethernet, USB, …

ALTERA FPGA for PCI
ALTERA FPGA for CAMAC

The pipeline CAMAC controller consists of a PC/104-Plus-based single board computer, PCI interface (PCI control) and CAMAC interface (CAMAC control).

Overview of Pipeline CAMAC controller (cont.)

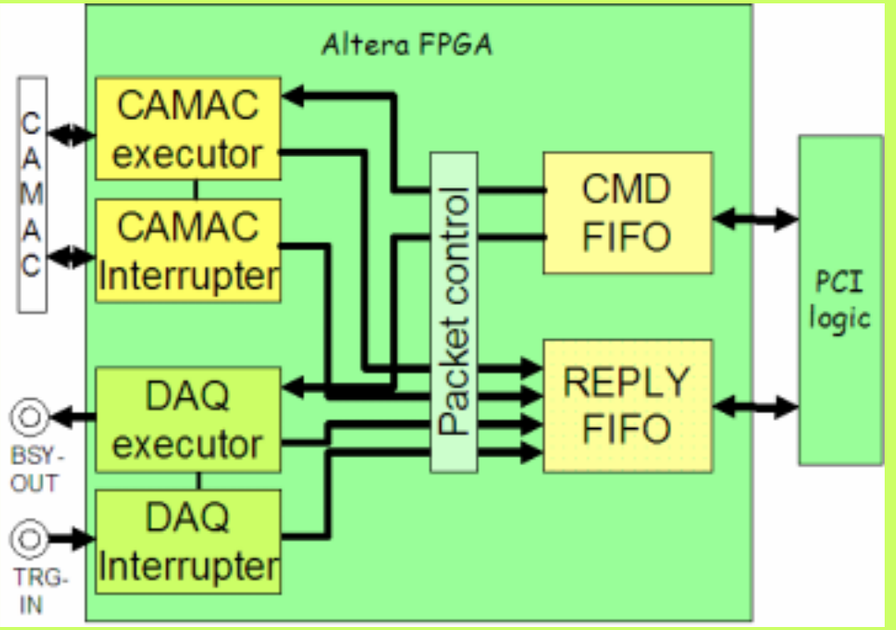
The PC/104-Plus is a standard PCI specification for embedded systems. Many PC/104-Plus based single board computers are available.

The PCI and CAMAC interfaces consist of an ALTERA FPGA, respectively . Those VHDL codes for the interfaces have been also developed.

The board computer adopted is Advantech PCM-9370, 3.5 inch (145 x 102 mm) Transmeta Crusoe 500 MHz processor single board computer including TM5400 processor, 320 MB memory, two IDE UltraDMA33 (with 512MB flash disk), LCD/CRT controller, 10/100 Mbps Ethernet controller, two 1.1 compliant USB ports, mini-din connector for keyboard, PS/2 mouse and so son. The power consumption is typically 10.7W.

Architecture of CAMAC control

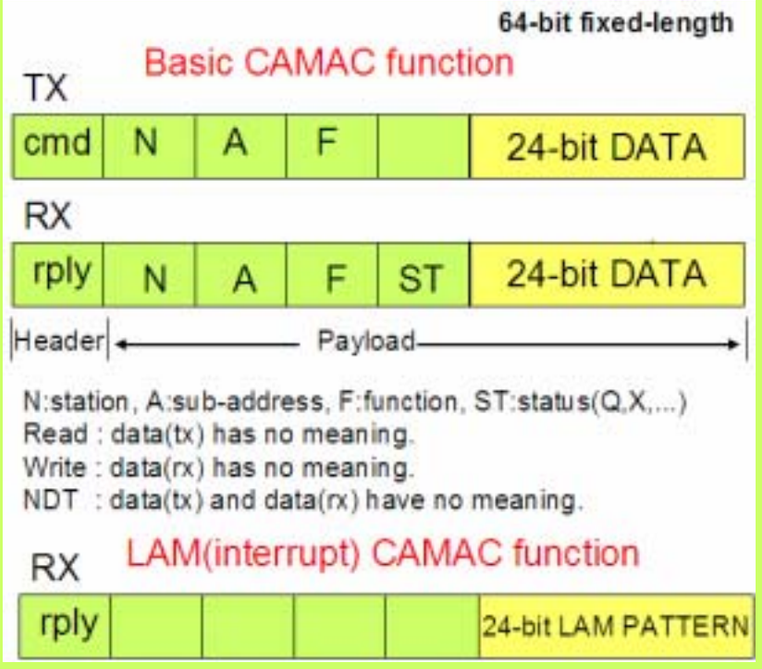
There are a CAMAC Executor, a CAMAC LAM Handler (CAMAC Interrupter), a DAQ Executor and a DAQ Trigger Handler (DAQ Interrupter). The Executors accept a packet including at least a command frame or more from CPU via PCI, execute them and then send reply frames to CPU. The frame is an unit of CAMAC access.

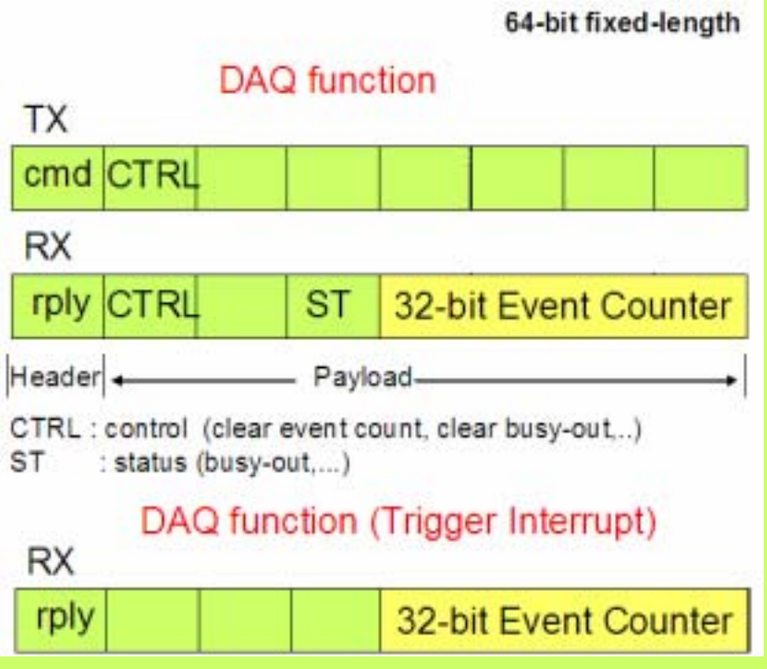


The pipeline CAMAC controller can execute CAMAC command with small overhead continuously by getting the command frames from a computer memory and then sending the reply frames to the computer memory, via PCI bus. The command FIFO and the reply FIFO have the size of 256 frames each. The Interrupters generate a packet including a reply frame and then send to CPU.

Frame format

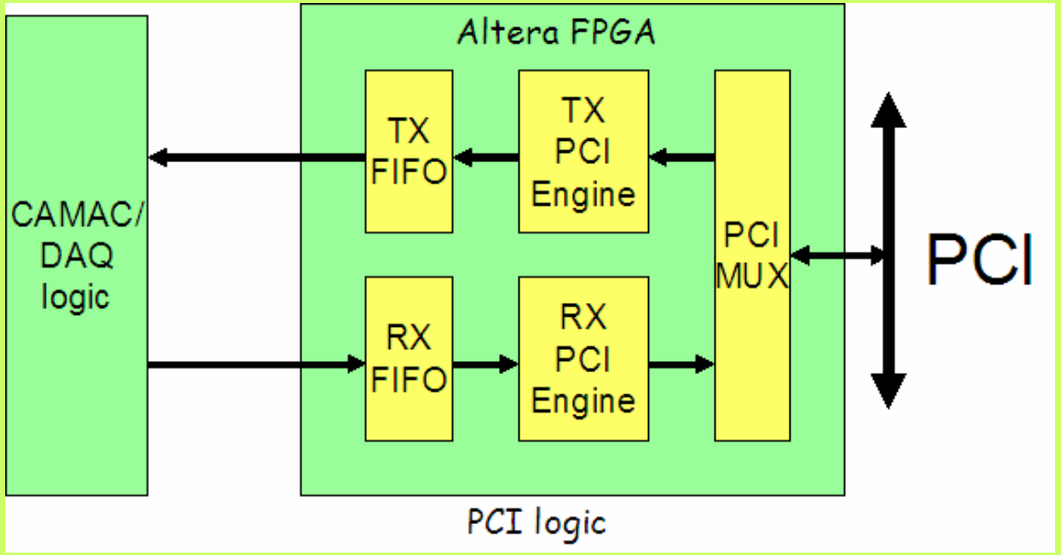
Command and reply frames have 64-bit fixed-length. It consists of an 8-bit header and a 56-bit payload. The payload for basic CAMAC command frame contains CAMAC station number N, CAMAC sub-address A, CAMAC function F and data to be written if necessary. That for the reply frame additionally contains CAMAC status such as Q & X and read data if the CAMAC function is read. That for CAMAC LAM includes 24-bit LAM pattern and that for DAQ Trigger includes 32-bit event count. DAQ executor can clear Busy-out signal while next event trigger is disabled.





Architecture of PCI control

There are, Tx/Rx FIFO, Tx/Rx engines and PCI multiplexer for Tx/Rx. Tx and Rx engines work independently while PCI multiplexer manages the PCI usage for Tx and Rx engines. Tx/Rx FIFOs have the depth of 256 with 32-bit width each.



The pipeline CAMAC controller sends multiple command frames, which include N, A, F and data if necessary, via Tx I/O registers. On the other hand, the controller receives multiple reply frames, which also includes N, A, F, status (Q and X) and data if necessary, via Rx I/O registers. The operations to Tx and Rx are done concurrently, independently, or asynchronously. If DMA is used in both sides, the throughput reaches maximum speed.

Operation and PCI I/O registers

The PCI I/O register map includes three kinds of registers. One is for Tx and another is for Rx. The other is system register. Those registers are located in PCI I/O space and the size of those registers is 32-bit.

In programmed I/O, data1 and data2 registers for Tx and Rx are used for sending command frames and receiving reply frames, respectively.

In block I/O, memory preset count register represents the number of frames in quad-word (8 bytes) to be transferred.

I/O offset address	Register name	Description
00h	TxData1	Tx data1 register
04h	TxData2	Tx data2 register
08h	TxControl	Tx control register
0Ch	TxStatus	Tx status register
10h	TxAddress	Tx memory address register
14h	TxPresetCount	Tx preset count register
18h	TxActualCount	Tx actual count register
1Ch	TxFifoCount	Tx FIFO count register
20h	RxData1	Rx data1 register
24h	RxData2	Rx data2 register
28h	RxControl	Rx control register
2Ch	RxStatus	Rx status register
30h	RxAddress	Rx memory address register
34h	RxPresetCount	Rx preset count register
38h	RxActualCount	Rx actual count register
3Ch	RxFifoCount	Rx FIFO count register
40h	System	System register

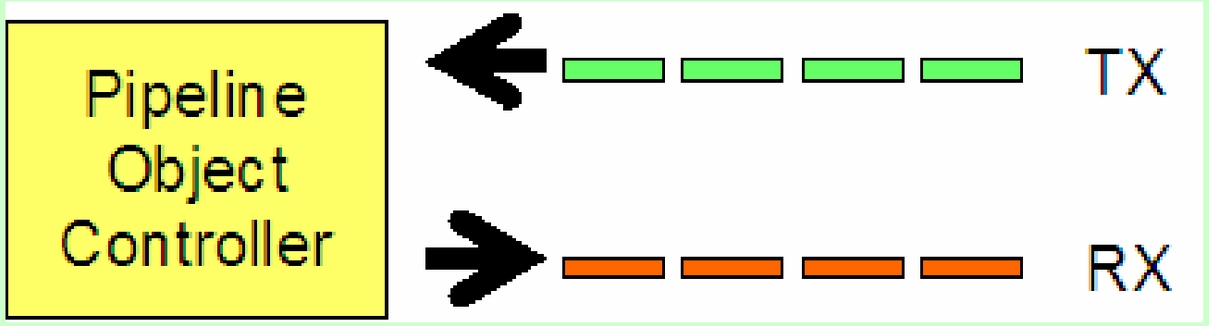
After the transfer is initiated by setting DMA-start flag, the actual count register counts the number of frames in quad-word (8 bytes) transferred actually.

Software

A Linux distribution kit tailored for the pipeline CAMAC controller is implemented on the PC/104-Plus single board computer while Linux is Open Source Software / GNU products, a commodity Open Source Operation System for PC compatible hardware.
The device driver and the library for the pipeline CAMAC controller have been developed. CAMAC and DAQ command frames are generated and then stored into a frame buffer by the frame generator. The command frames in a frame buffer are executed by Programmed I/O routines, Block I/O routines or the combined routines in same manner. The reply frames are stored into another frame buffer as result of the command frame executions. The reply frame includes CAMAC status and data. The extractors of the status and the data from the reply frames are provided. The wait routines for LAM interrupt and Trigger interrupt are also available.

Design Concept

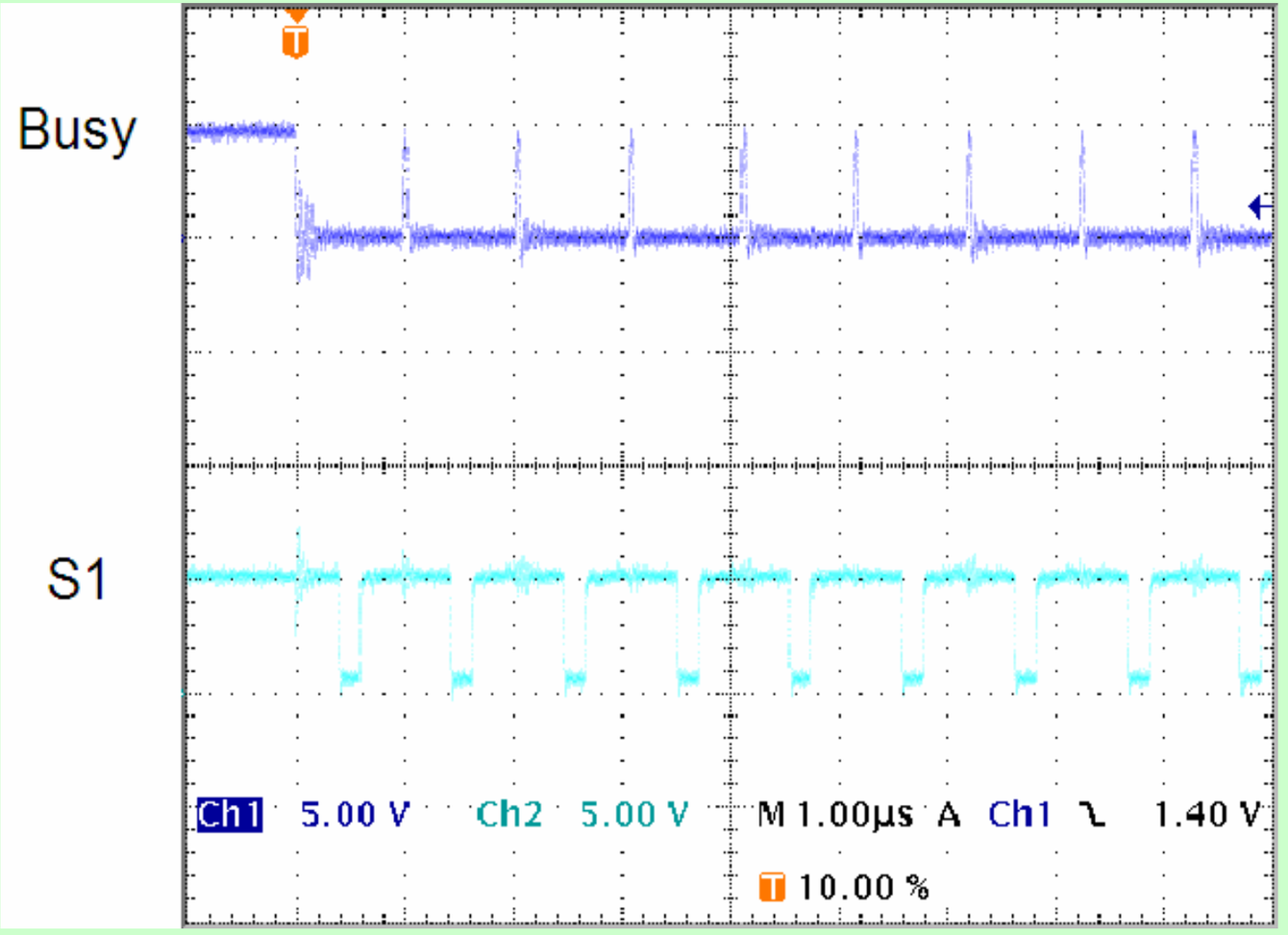
The pipeline CAMAC controller adopted truly pipelined command and data paths from/to computer memory to/from CAMAC.



The pipeline method enabled the controller maximum speed of CAMAC access, approximately up to 3 MB/sec with 24-bit data. In the pipeline method, the multiple command frames and the multiple reply frames are processed asynchronously, independently or concurrently. The pipeline method is best for the speed up of I/O throughput. The method is generally usable, namely, as the access method to I/O object controller, which includes not only CAMAC but also readout equipment such as Flash ADC.

Performance

CAMAC executor executes a CAMAC command frame in 1.04 usec. The horizontal axis is timing in unit 1 usec. Each CAMAC cycle is continuously done in 1.04 usec The speed was achieved by the DMA operation.
In fast mode which ignores CAMAC S2 timing signal, it executes the command frame in 0.72 usec.



CAMAC timing

Conclusions

- A pipeline CAMAC controller with new architecture has been developed.
- The CAMAC access speed reached up to maximum speed of CAMAC, approximately 3 MB/s with 24-bit data.
- The pipeline method will be useful for not only CAMAC controller but also other controller, generally, I/O object controller.

References

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