Super KEKB Data Acquisition System

Mikihiko Nakao (KEK)

5 October, 2001

at the Electronics/Online Users’ Workshop

RECENT BELLE RESULTS

$\int \mathcal{L} = 29.1\text{fb}^{-1} \Rightarrow$ 32M $B\bar{B}$ events — recorded by July 2001

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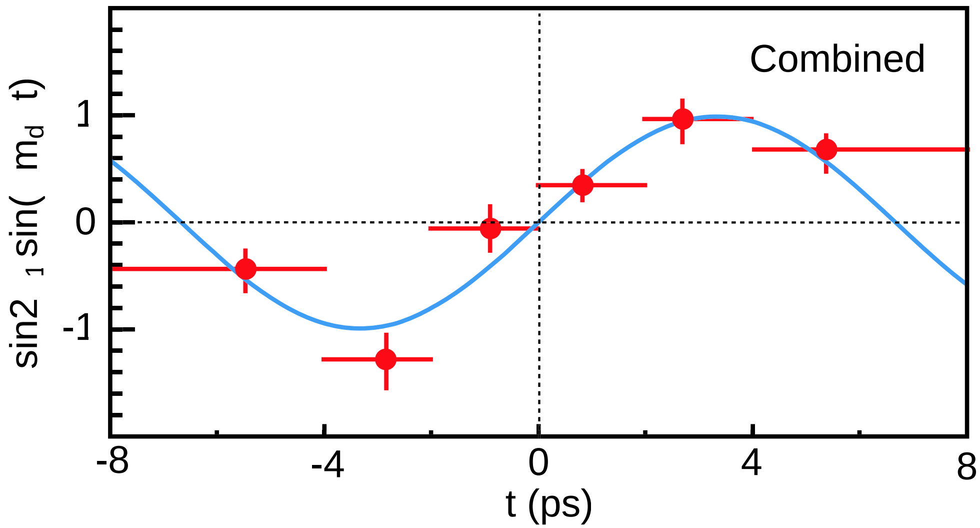
Observation of CPV in B decay



$$\sin 2\phi_1 = 0.99 \pm 0.14 \pm 0.06 \quad (\neq 0)$$

First step towards
CKM unitarity triangle

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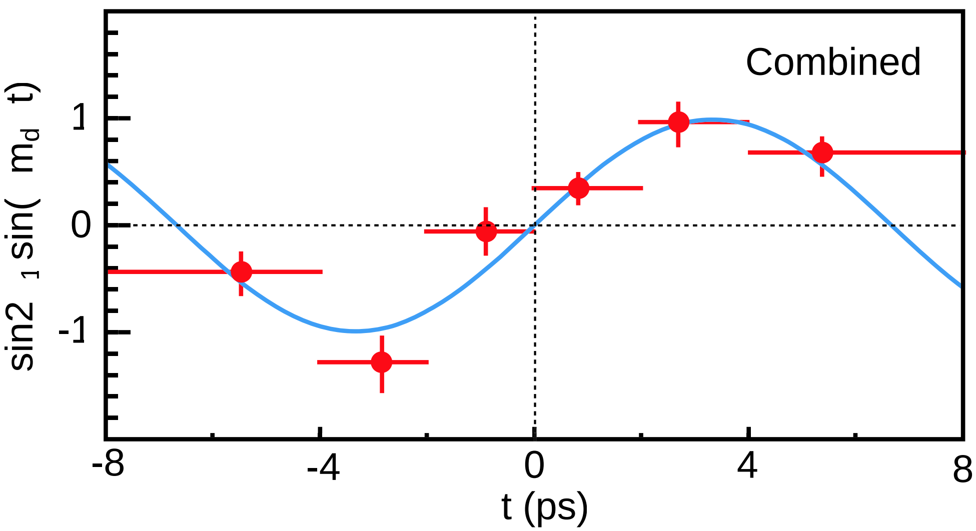

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First step towards
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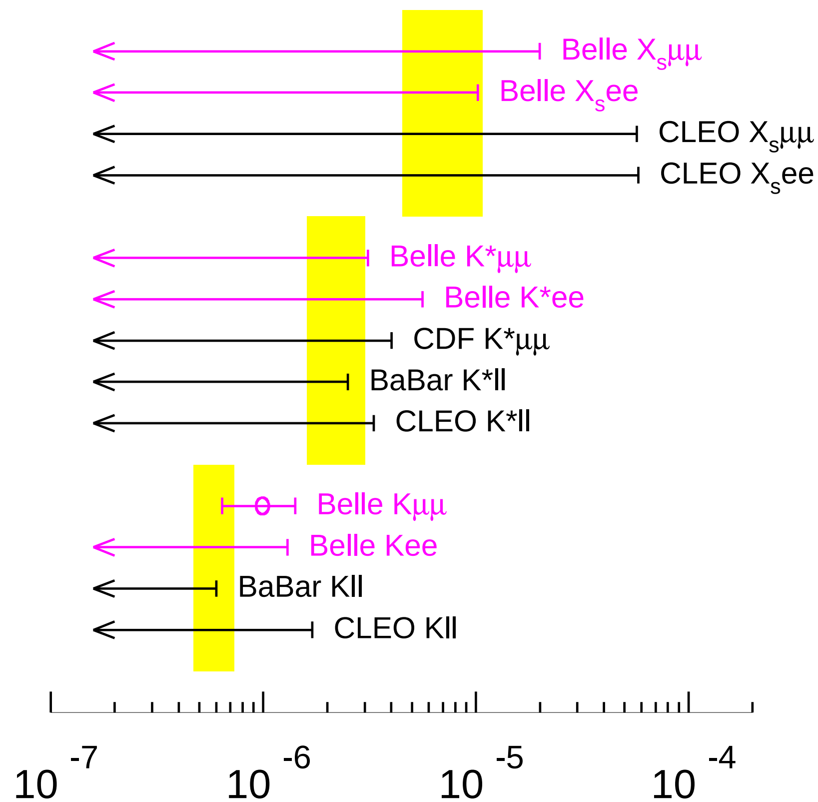
Observation of $B \to K\mu^+\mu^-$ decays



First step on
very rare decays as BSM probe

- Activities
  - Just started — first workshop in Aug. 2001
  - (note: none of these activities / plans are official yet)

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- Motivation — Flavor physics
  - Beyond the precision Measurement of CKM matrix
  - Tool to understand the physics of higher energy and beyond SM (BSM)
    — *As kaon experiments have been.*
  - Complementary to the energy frontier experiments (LHC, LC, . . .)

SUPER KEKB

▷ Activities

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▷ Motivation — Flavor physics

▷▷ Beyond the precision Measurement of CKM matrix

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▷▷ Complementary to the energy frontier experiments (LHC, LC, . . .)

▷ Solution — Luminosity frontier

▷▷ Upgrade KEKB and Belle for $\mathcal{L} = 10^{35}$ cm^{-2}s^{-1} ($\times 10$ of the current design)

▷▷ e^+e^- experiment is better in many channels than hadron machines

— (BTeV, LHCb, ATLAS, CMS)

ROADMAP

First Step

Discovery of CPV
in B-decay

$$\int \mathcal{L} = 30\ \mathrm{fb}^{-1}$$

$$\mathcal{L} = 4.5 \times 10^{33}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$$

2001 (Now)

Achieved

ROADMAP

First Step

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$\int \mathcal{L} = 30\ \mathrm{fb}^{-1}$
$\mathcal{L} = 4.5 \times 10^{33}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
2001 (Now)
Achieved

Second Step

Precision test
of KM Model

$\int \mathcal{L} = 300\ \mathrm{fb}^{-1}$
$\mathcal{L} = 1 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
2005
Current KEKB and Belle

ROADMAP

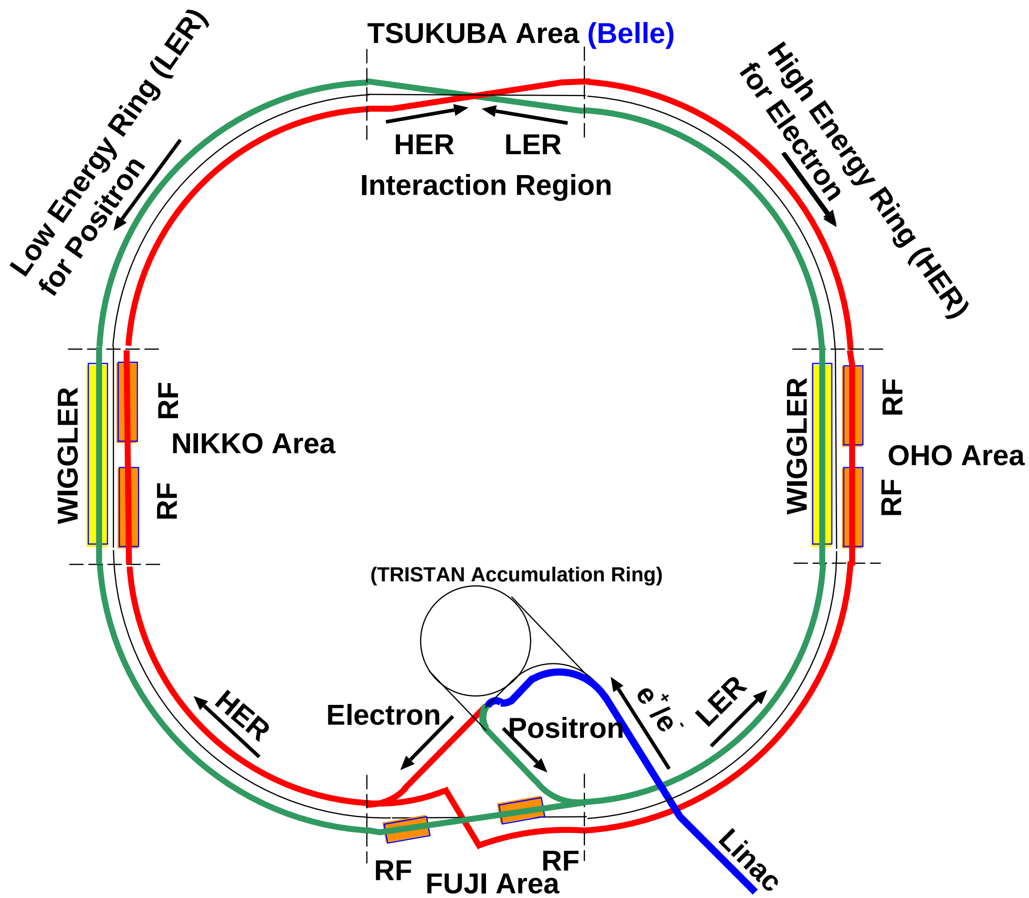
First Step	Second Step	Third Step
Discovery of CPV in B-decay	Precision test of KM Model	Flavor physics on BSM
$\int \mathcal{L} = 30\ \mathrm{fb}^{-1}$	$\int \mathcal{L} = 300\ \mathrm{fb}^{-1}$	$\int \mathcal{L} = 3000\ \mathrm{fb}^{-1}$
$\mathcal{L} = 4.5 \times 10^{33}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$	$\mathcal{L} = 1 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$	$\mathcal{L} = 10^{35}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
2001 (Now)	2005	2010?
Achieved	Current KEKB and Belle	Super KEKB

OKADA MATRIX

		—SUSY—		$\not R$	W_R	extra	2HDM	extra	
	mSUGRA	Minimal Flavor Mixing	General Flavor Mixing	SUSY	Z'	quark	MHDM	dim.	...
B_d Unitarity triangle									
$b \to s\ell^+\ell^-$ inclusive									
$B \to K^{(*)}\ell^+\ell^-$									
$b \to s\tau^+\tau^-$									
$B \to K^{(*)}\nu\bar{\nu}$									
$b \to s\gamma$ direct asymmetry									
$B \to K_1\gamma$ indirect asymmetry									
$b \to d\gamma$									
$B \to \rho\gamma$									
$B \to D^{(*)}\tau\nu$									
$B \to \tau\nu$									
$B \to \phi K_S$									
⋮									
⋮									

Sensitivity studies in progress

Accelerator Upgrade

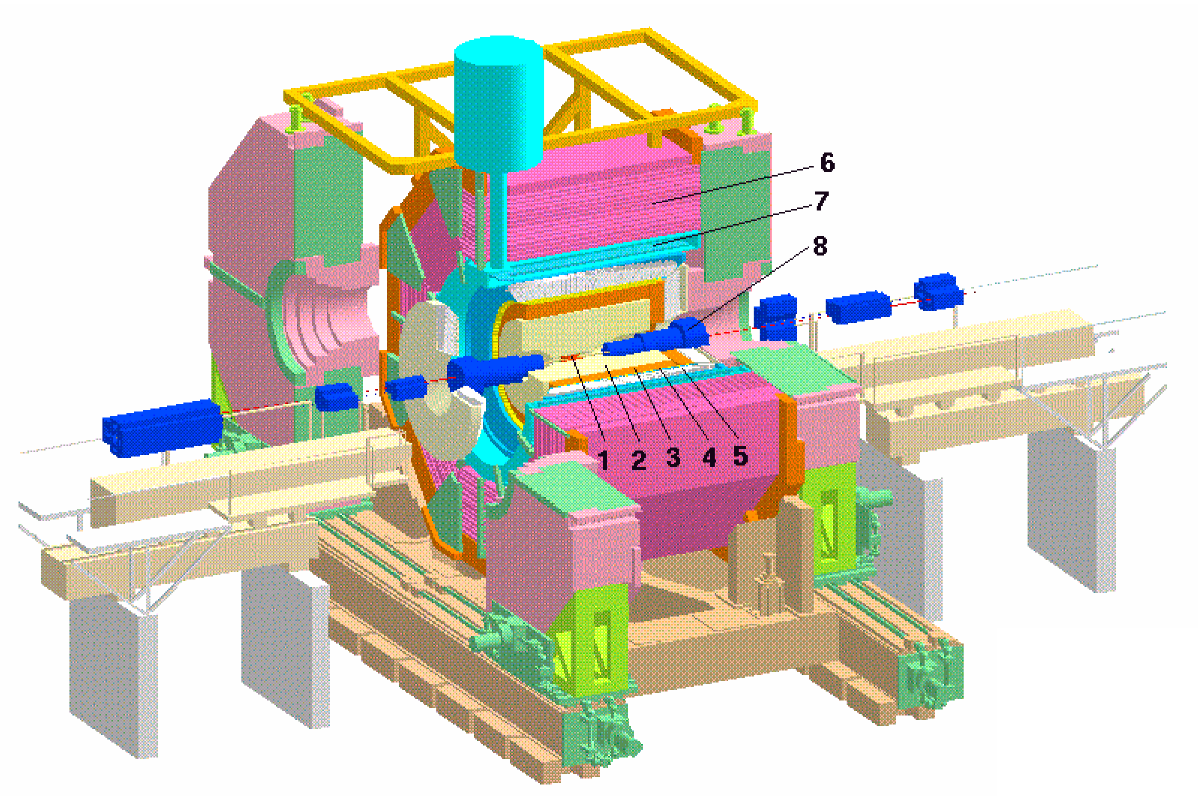


- More beam current
  0.9 A/0.8 A $\rightarrow$ 10 A / 3 A (LER/HER)
- Squeeze beam more
  - Squeeze β_y^* : 6.5 mm $\rightarrow$ 3 mm
  - Bunch length 5 mm $\rightarrow$ 3 mm
- New IR design
  - Crossing ± 11 mrad $\rightarrow$ ± 15 mrad
  - Crab cavity
- Electron cloud
  - Swap $e^+ \Leftrightarrow e^-$
  - Ante-chamber

IR UPGRADE

- ▷ New interaction region (IR) design is needed.
- ▷ QCS (final focus quad) closer to IP — No EFC (extreme forward calorimeter)
- ▷ Beam mask design is essential for radiation tolerance, cooling design, and beam background estimation.
- ▷ Aiming for 1.0 cm radius beampipe (for better vertexing) Beam-pipe with 1.5 cm radius is OK.

BELLE DETECTOR



1. silicon vertex detector (SVD)
   3 layers of double sided sensors
2. central drift chamber (CDC)
   50 anode layers
3. aerogel cherenkov counters (ACC)
   1188 cells, $n = 1.01$ to 1.03
4. time-of-flight counters (TOF)
   4cm thick scintillator, 128 in ϕ
5. electromagnetic calorimeter (ECL)
   8736 CsI(Tl) crystals
6. K_L and μ detector (KLM)
   14 layers of glass RPC in iron yoke
7. superconducting solenoid
   1.5 Telsa
8. extreme-forward calorimeter (EFC)
   320 BGO on top of final focus quad

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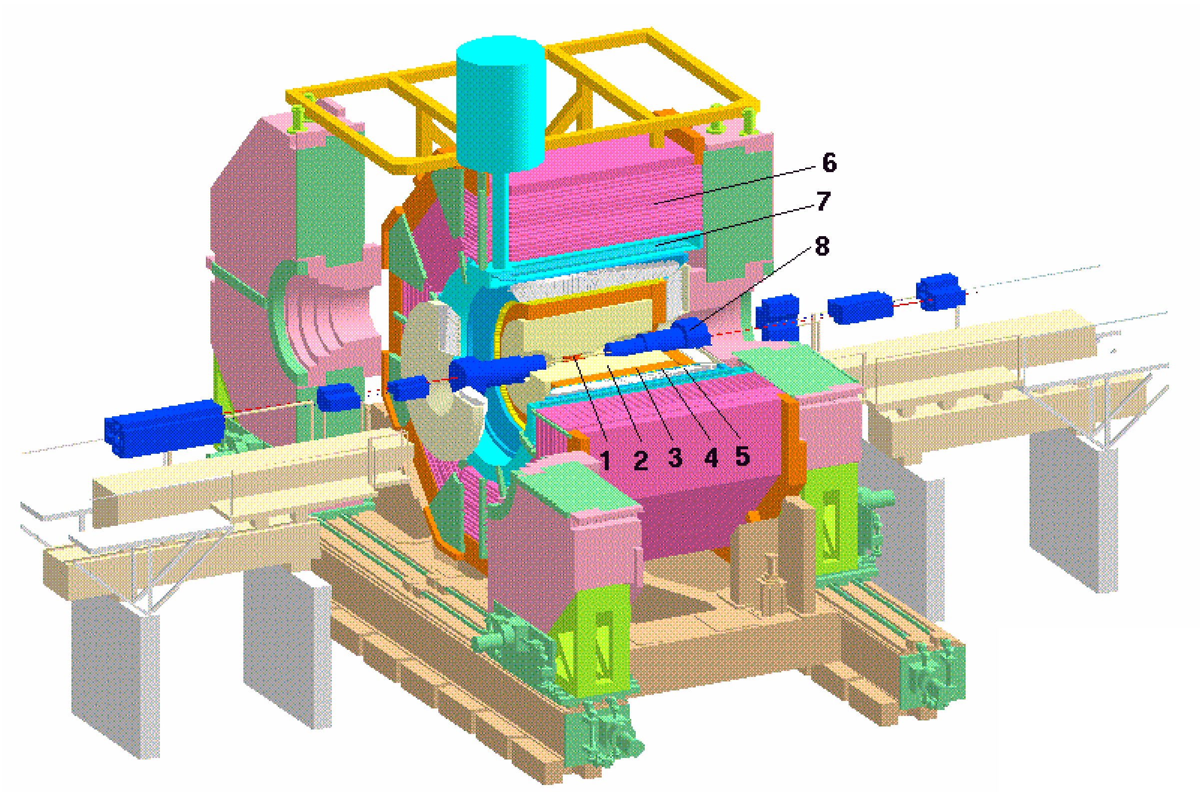

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- ▷ Physics goal
- ▷ Radiaion tolerance
- ▷ Occupancy
- ▷ Readout deadtime

DAQ35 DESIGN SPEC

	4×10^{33} cm^{-1}s^{-1} (now)	1×10^{35} cm^{-1}s^{-1} ($\times$25)
More background	200 Hz (design: up to 500 Hz)	1 - 3 kHz (?) ★1 (design: up to 5 kHz)
More physics	40 Hz (BB+qq: 15 Hz)	1 kHz (!) (BB+qq: 400 Hz (!))
Data size	40 kB (SVD: 15 kB)	100 kB ★2 (pixel SVD: 50 kB)
Data flow at L1	10 MB/s (design: 15 MB→40 MB) ★4	200 - 400 MB/s (design: 600 MB/s (!))
at storage	5 MB/s (design: 15 MB→24 MB) ★4	50 - 100 MB/s ★3 (design: 240 MB/s)

★ 1 Background rate should not scale to luminosity... probably scale to the beam current.

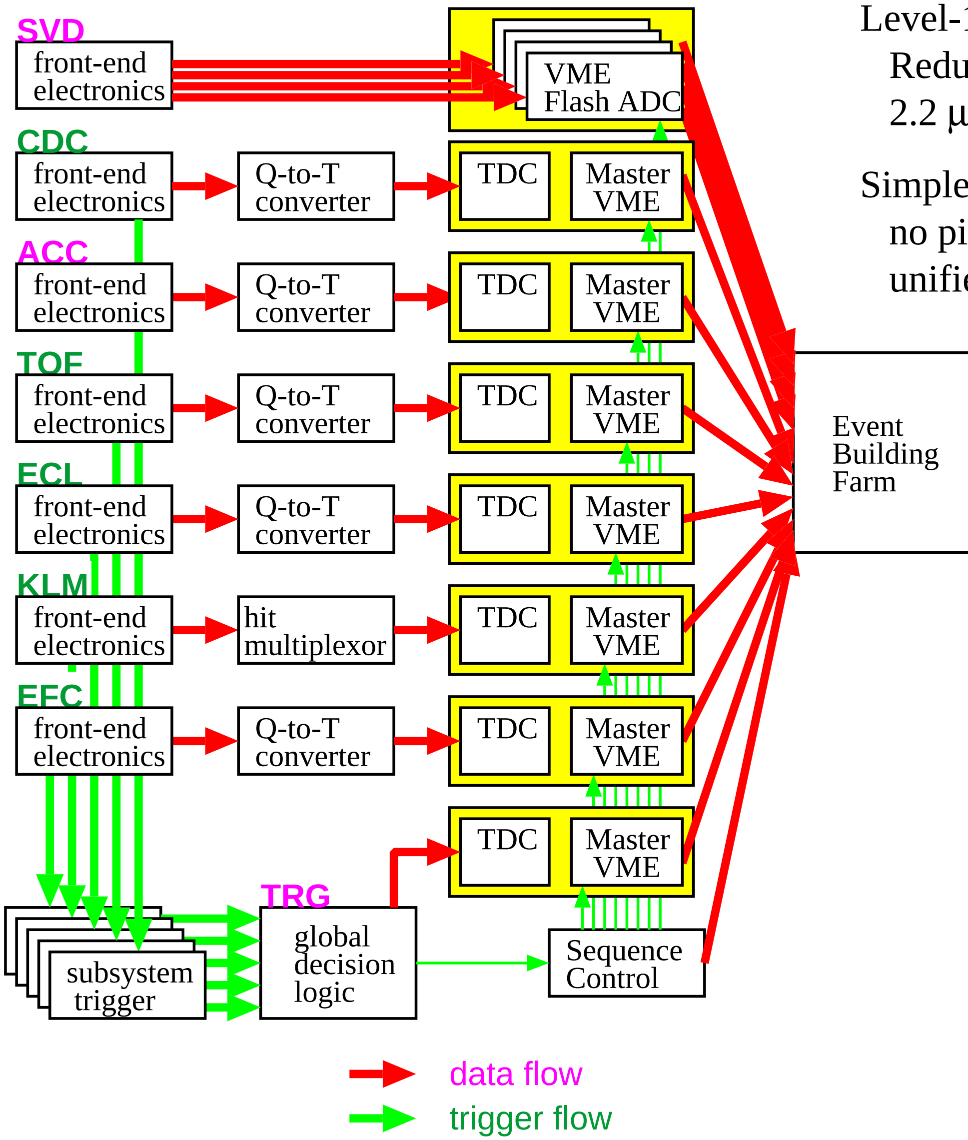
★ 2 Data size will increase due to a larger occupancy.

★ 3 A factor of 2 more reduction with software trigger, prescaling two-photon/ττ/μμ/eeγ.

★ 4 After DAQ upgrade in summer 2001 (now)

ELECTRONICS AND DAQ NOW

- ▷ Front-end system since beginning
- ▷ New event building farm + data storage system just replaced



Basic features of Belle trigger/DAQ

Level-1 trigger
- Redundant triggers (track/neutral)
- 2.2 μs latency

Simple and robust DAQ
- no pipeline readout
- unified TDC readout with Q-to-T

Basic specifications

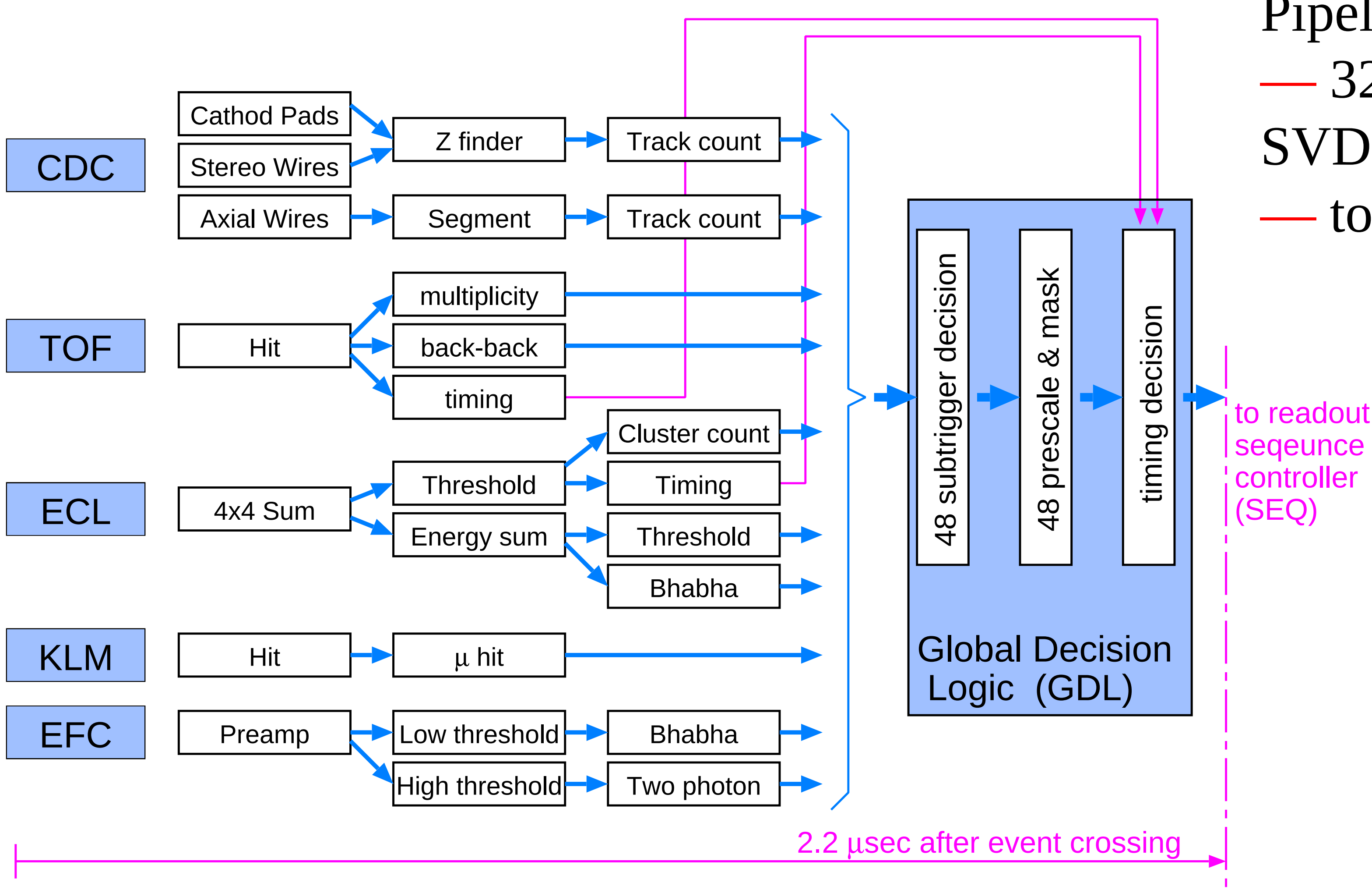
200 Hz L1 trigger rate
(500 Hz maximum)

30 KB/event (15 MB/s),
down to the tape

<200 μs deadtime
(<10% at 500 Hz)

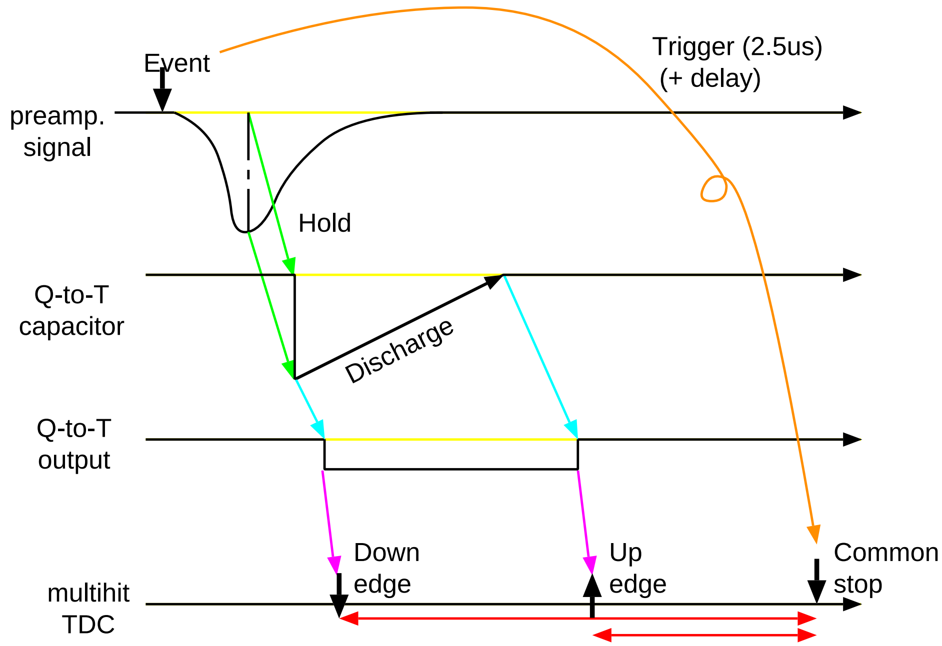
L1 TRIGGER NOW

Level-1 trigger

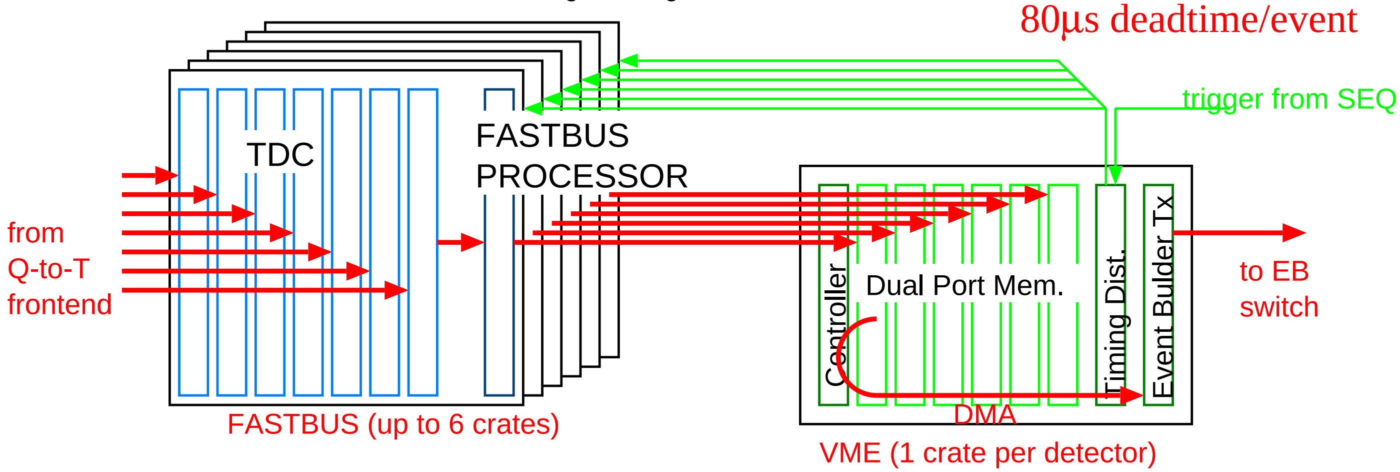


Pipelined
— 32/64 MHz clock
SVD trigger
— to be added soon

Q-TO-T + FASTBUS SYSTEM NOW



Two timings are digitize and read out.



Q-to-T (charge to time) converter

LeCroy MQT 300A Q-to-T chip
CDC / ACC / TOF / ECL / EFC

TDC readout

LeCroy LRS1877S FASTBUS multihit-TDC
built-in sparsification function
CDC / ACC / TOF / ECL / EFC / KLM / TRG

KLM : hit map is serialized
TRG: all the timings are recorded

Unified VME readout system

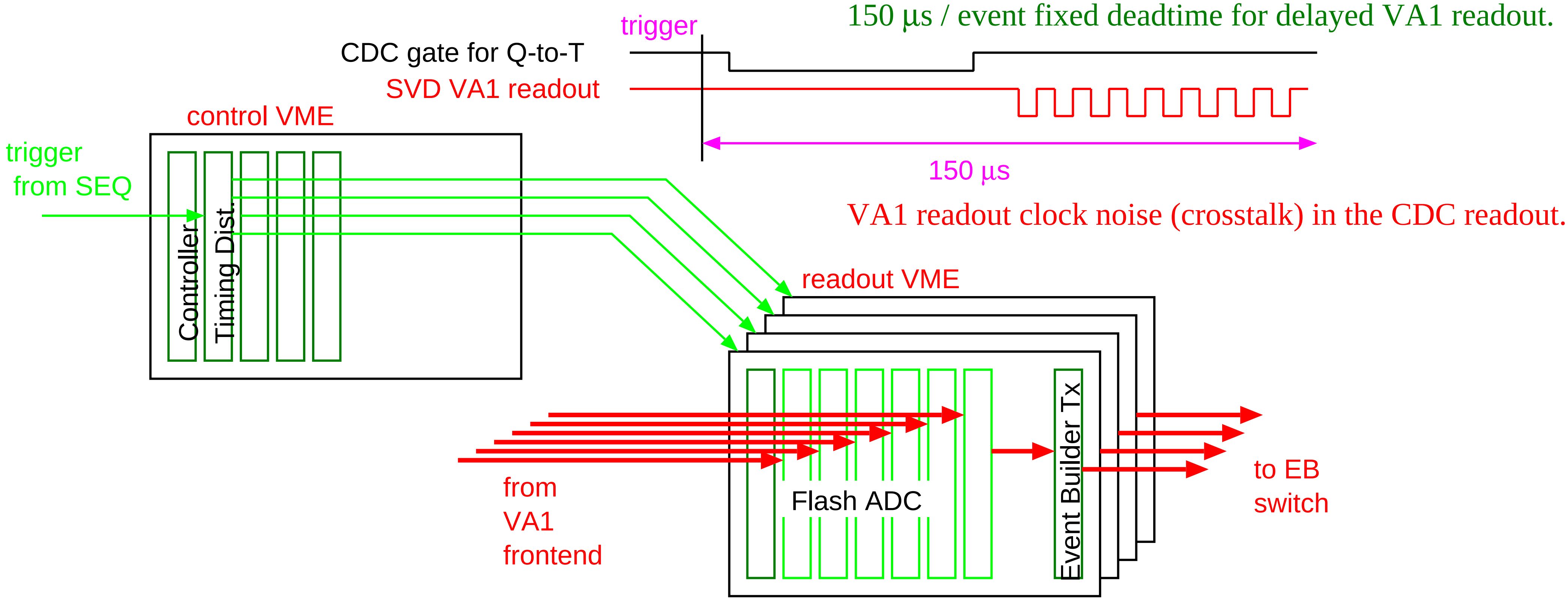
Motorola MVME162(VxWorks) controls
Homemade FASTBUS/VME interface with DPM.
The same software for all the TDC systems
5.5 MB/s TDC readout / 3.5 MB/s to Event builder
80μs deadtime/event

VA1 + FADC SYSTEM NOW

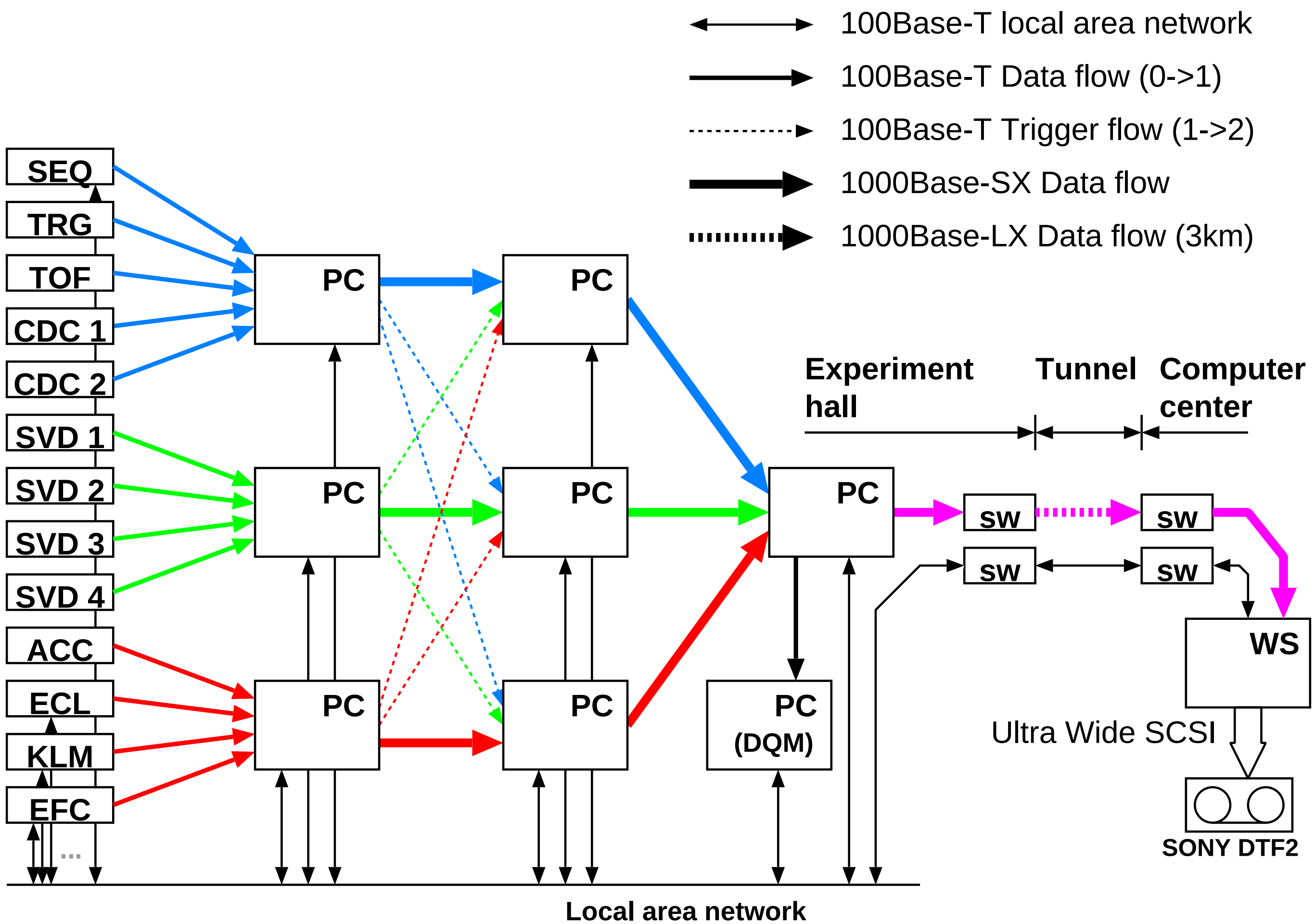
Flash ADC to readout frontend VA1-chip

sparsification by onboard DSP
4 VME crates to readout flash ADC

VA1 latch at 1μs by the TOF cluster pre-trigger (a few kHz)



Event Building Farm now



layer 0
VME readout

layer 1
partial event building + level-2 reconstruction

layer 2
level-2 filtering

layer 3
final event building + level-3 filtering

layer 4
mass storage

Switchless EB-farm from 2001 fall

first physics run from today!

- layer0 → 1 — 5 MB/s/link
- layer1 → 2 — 15 MB/s/link
- layer2 → 3 — ∼50% reduction
- layer3 → 4 — 24 MB/s

ELECTRONICS FOR SUPER KEKB

Current DAQ system will not work with 10 times higher background rate.

At 5 kHz, deadtime $< 10\mu$s is needed.

▷ L1 latency (2.2 μs) is too long if trigger comes at 5 kHz.
Need pipeline buffer (analog/digital) before L1 decision.

▷ No software based readout system.
Need large FIFO buffer (with sparcification) for a delayed readout.

▷ Individual systems:

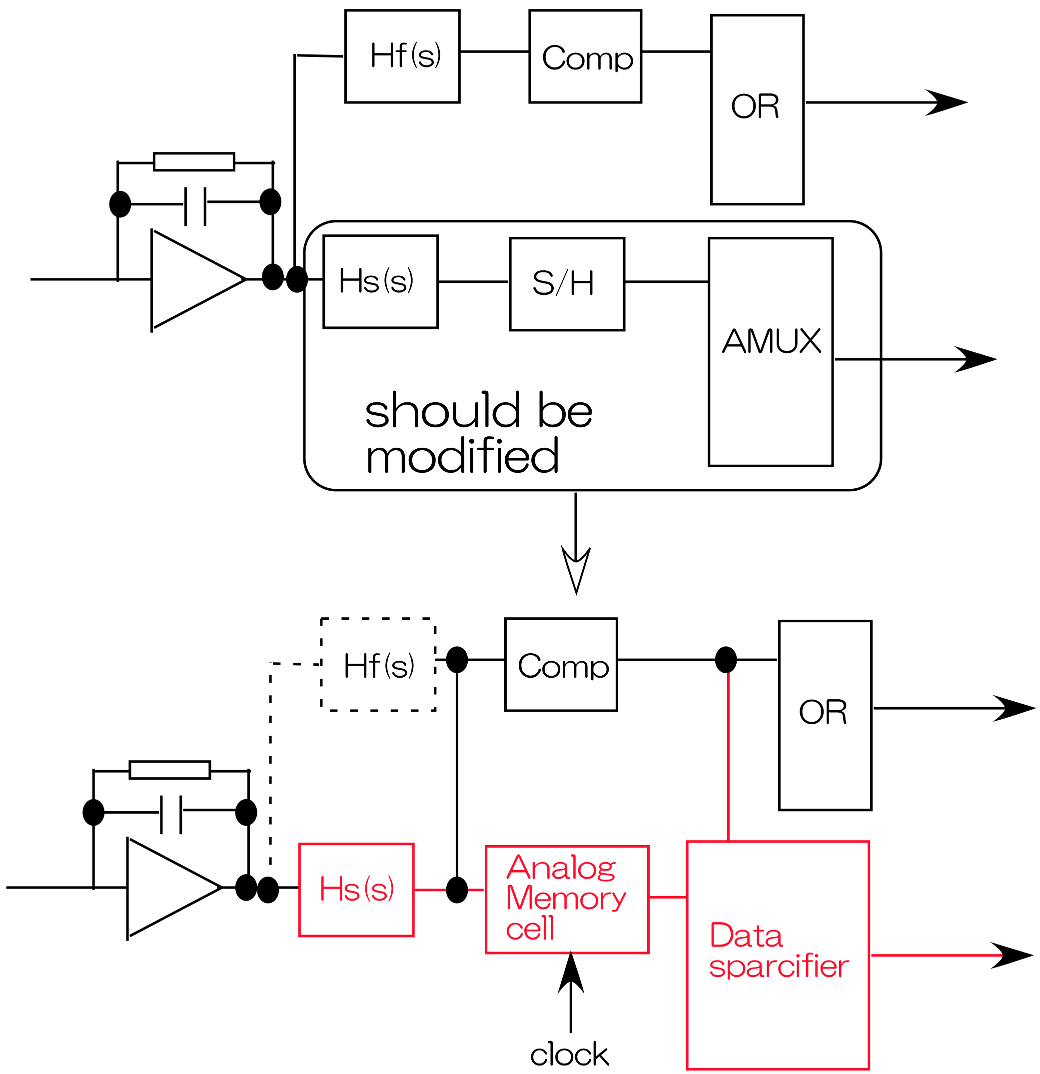
▷▷ SVD — Occupancy will be critical (4% $\rightarrow$ 40%?)
Analog pipeline should be in front-end

▷▷ ECL — Need faster shaping time
Pileup effect

▷▷ CDC — Inner part should be replaced with SVD.
dE/dx measurement. (similar system for PID/KLM).

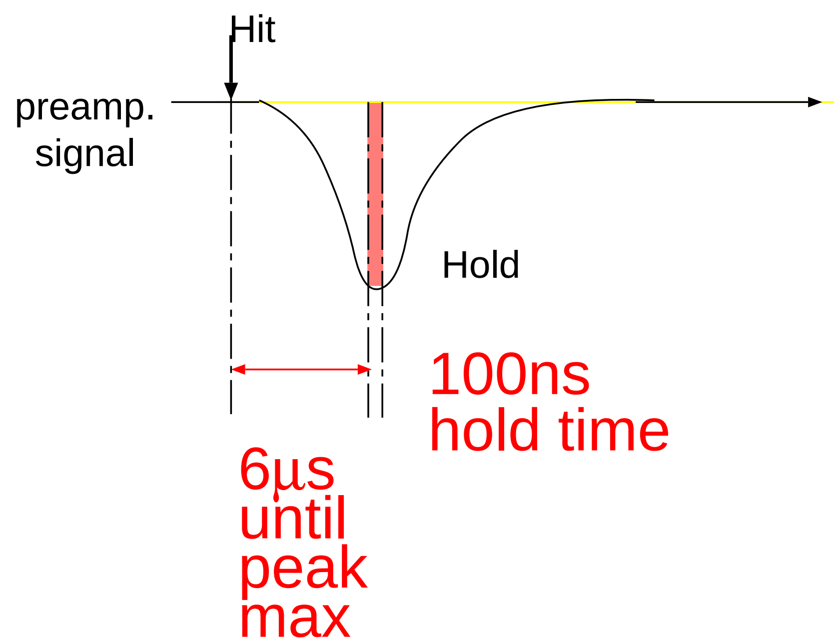
SVD ELECTRONICS

- Closely related to the new SVD design
(vertex resolution, occupancy, radiation tolerance, cost, . . .)
- Pixel or not — finer innermost layer to reduce occupancy
- Extended outer layer — drift chamber will not work there
- Analog pipeline on the readout chip — not so easy task



ECL ELECTRONICS

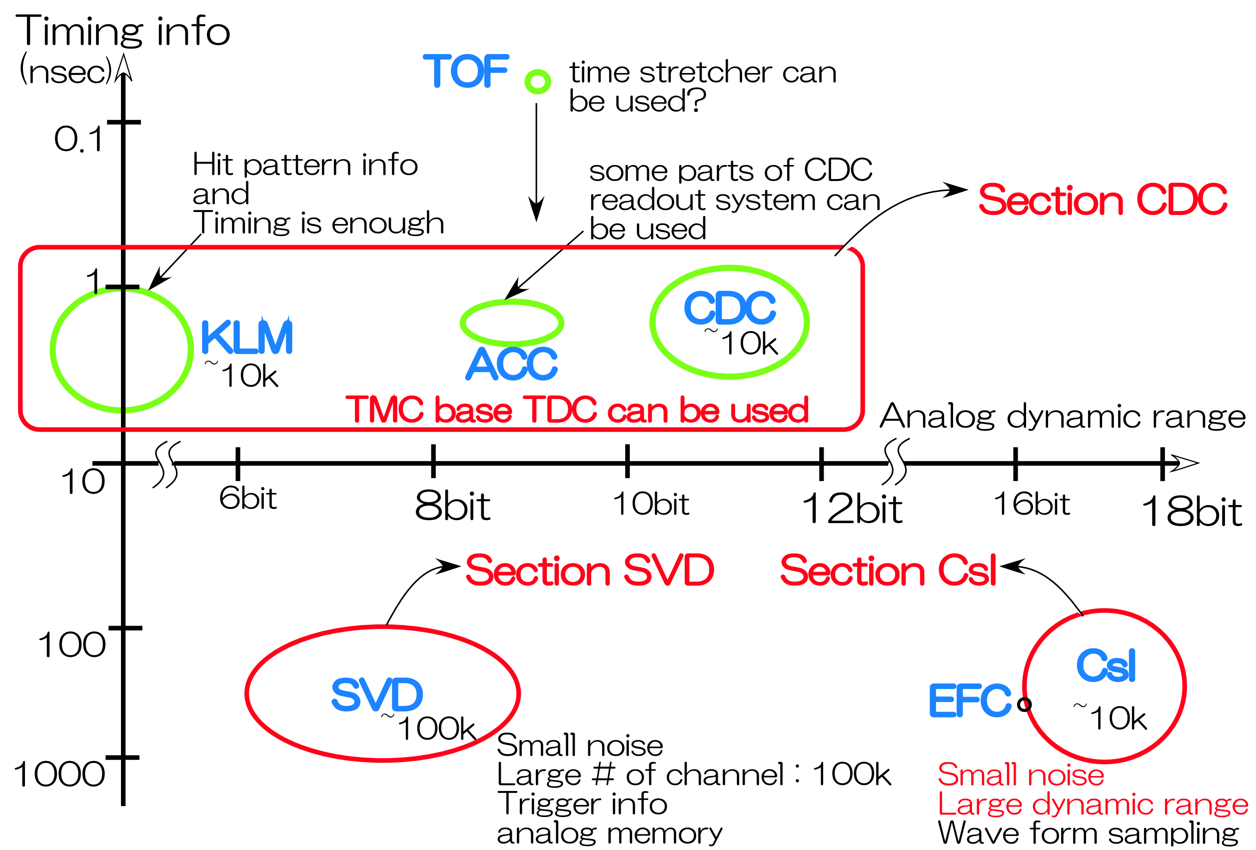
- Use the same CsI(Tl)
  — OK in terms of radiation
  (too costly to find and replace with a new/better crystal)
- The optimal shaping time is too slow, if pile up is considered.
- Lots of low energy pile-ups
  (a few MeV $\rightarrow \Sigma \sim \mathcal{O}(\mathrm{GeV})$).
- Need much shorter shaping
  multi-range flash-ADC
  + waveform sampling.



1μs shaping time
$\rightarrow$ 6μs peak time
$\rightarrow$ 2 MeV equiv. pile up

CDC electronics

- ▷ Use similar drift chamber — OK in terms of occupancy.
- ▷ TMC (time-memory chip) is a good candidate for readout.
- ▷ dE/dx should be carefully considered.
- ▷ Similar readout can be used for PID and KLM (but a new PID detector may have to be rebuilt).



ELECTRONICS SUMMARY

almost of all detectors should be redesigned

	hit rate/ch or occupancy			typical time scale of detector	detector @ x100
	present	x10	x100		
KLM	B:4Hz E:>40Hz	B:40Hz E:>400Hz	~5kHz	1msec/cm^2 (op-mode)	<1/10:op-mode & electronics <1/factor:segmentation
CsI	σ noise	<3σ noise	<10σ noise	>900nsec	
TOF	30kHz	300kHz	3MHz	~50nsec	<1/50:segmentation&electronics
ACC	B:1kHz E:5kHz	10kHz 50kHz	100kHz 500kHz	~50nsec	<1/10:segmentation
CDC	5kHz* w/o inner	50kHz <10%	500kHz	~400nsec (cell size)	
SVD	20kHz 4%	40%	100%	0.1~1μsec (noise)	even if x10 fine granularity is necessary
EFC					

Deadtime fraction of most detectors > 5%

DAQ BACKEND

- Readout system
  - Non-VME system can be used if realtime software is not needed.
    - Serial line readout (USB2.0 or IEEE1394)
- EB-farm
  - No much room to add EB-farm nodes to cope with $\times$10 data rate.
    - Event distribution and multiple EB-farms running in parallel.
- Storage system
  - No single drive can write at a rate of $\times 10$ data rate.
    - Disk caching and delayed writing into multiple tape drives.

Readout Unit

Readout Unit

1 PC + 1 box + 1 timing system

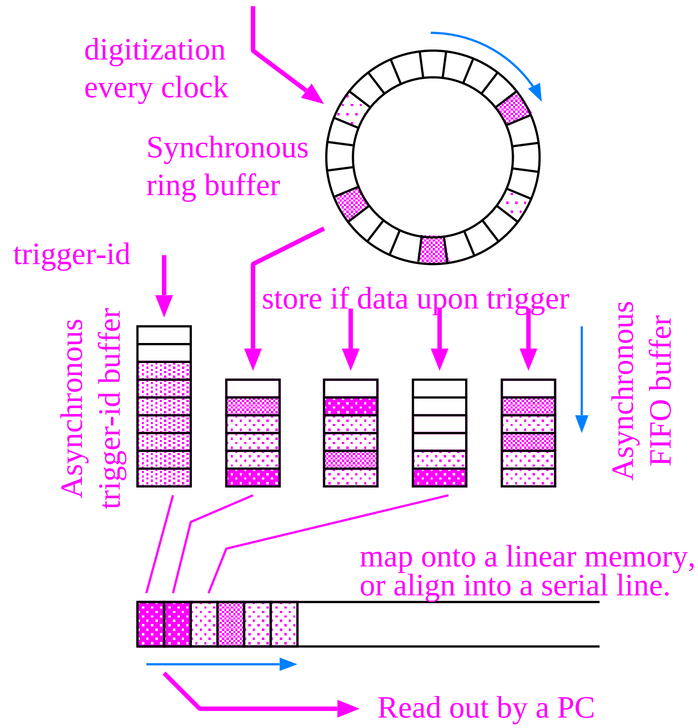
Backplane system (9U VME?)
is convenient for misc. purposes.

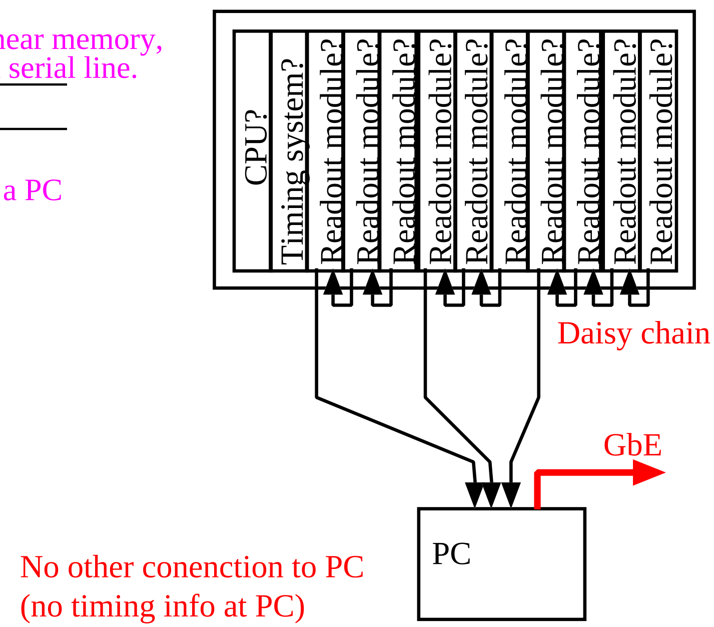
Data readout/transfer
using serial-bus
(USB2.0 or IEEE1394).

10-20 readout module / crate

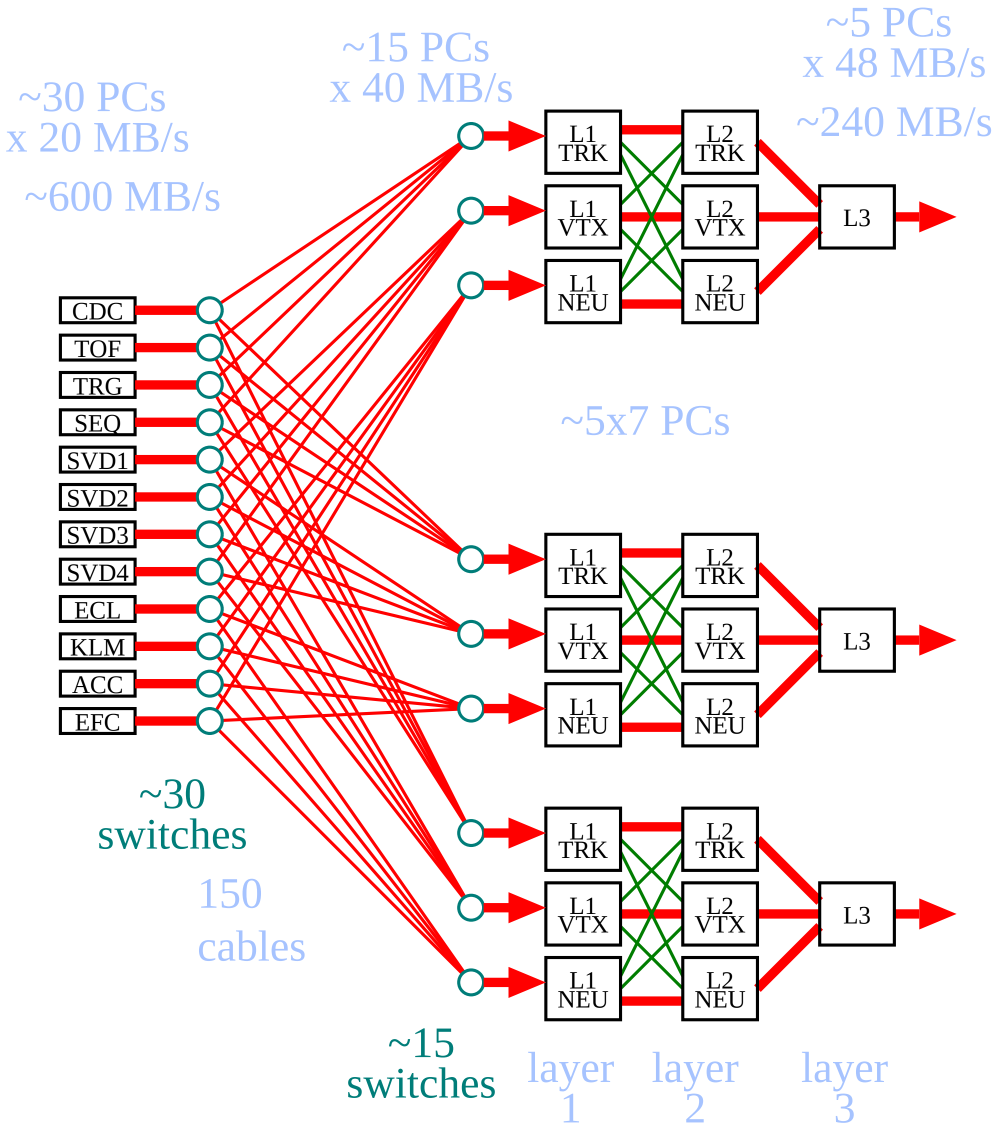
~1-2K channel / unit for ECL / CDC
~10-20K channel / unit for SVD

10-20 MB/s (5kHz) throughput





MULTIPLE EB-FARM



One of the possible configuration,
with no much challenge for per-node speed.

1-to-5 splitting (GbE to FastE) and
10-to-1 bundling (FastE to GbE),
with inexpensive network switches.

Scalable up to 1-to-N (N~O(10)) splitting

May need some network techniques
such as QoS (RSVP) and/or VLAN.
(need to confirm).

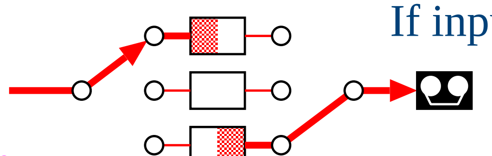
DISK CACHING

Tape drive candidates:
SONY DTF3 (48 MB/s) in 2002
DTF4 (96 MB/s) in 2006?

⇒ No single drive at 240 MB/s
No data transfer, either?
Disk cache and delayed write

Switching disks

Need multi-port disk ?
PC with multi-port
network + network switch



If input speed = output speed, 3 PC is enough

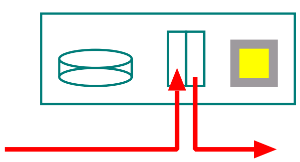
If input speed = N * output speed, N+2 PC are needed

If 10 PC for 5 drives, disk-to-tape connections are fixed, and some margin for storage is provided.

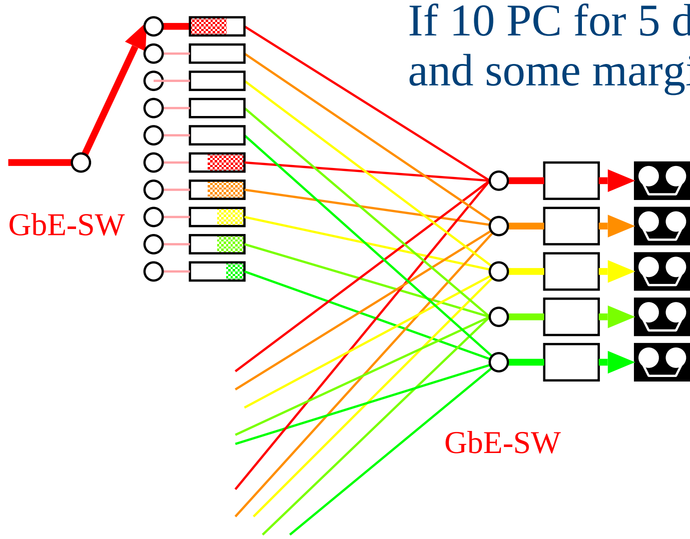
Unit PC for disk caching

200 GB
~50 MB/s

2-port
x GbE



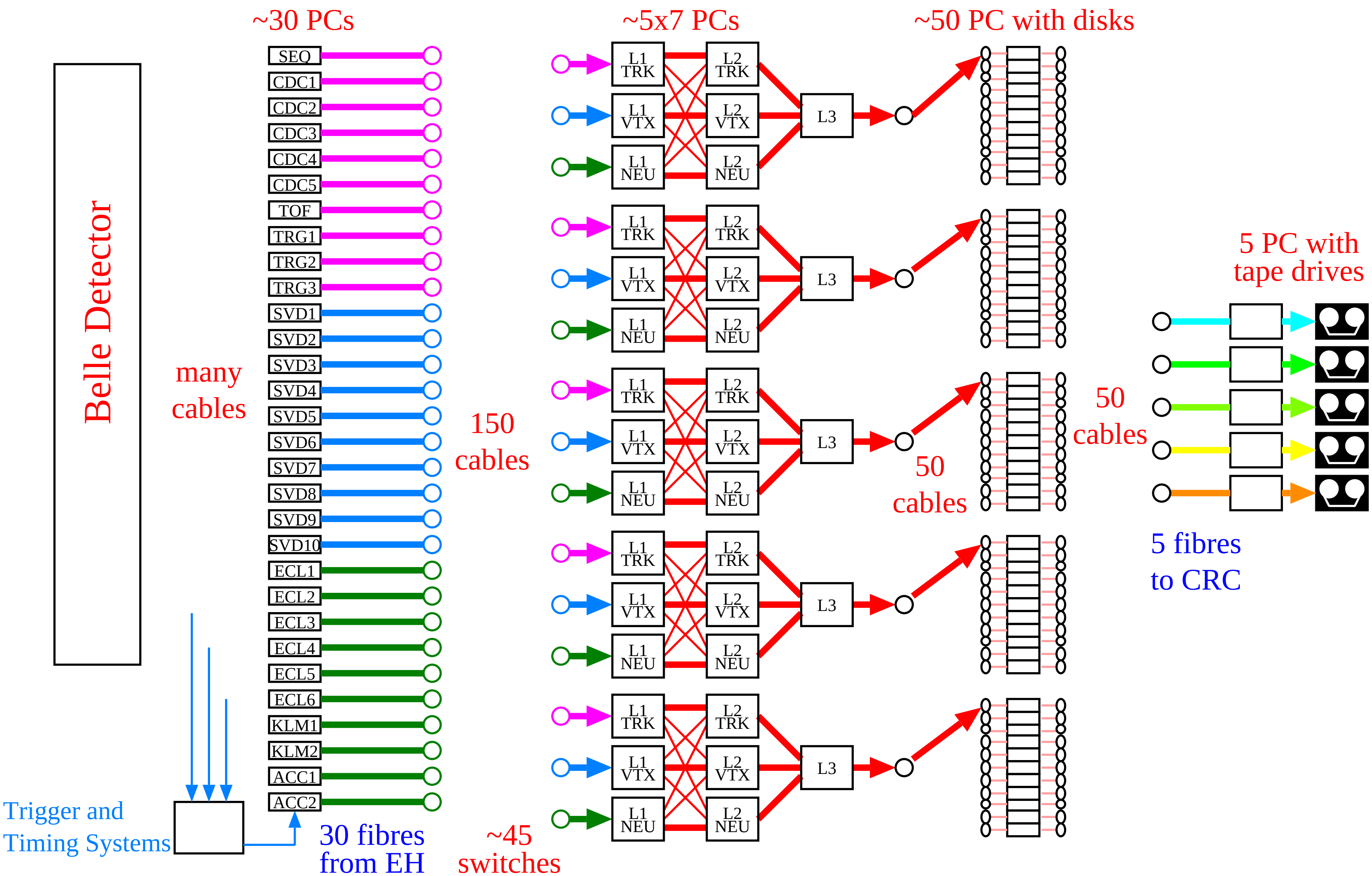
Fast enough disk? If not, RAID?



x50 PC (200 GB disk/PC)

x10 1-to-10 full GbE SW

DAQ35 FULL CONFIGURATION



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    So far, and so will be.